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Single Event Upset and Latchup Considerations for CMOS Devices Operated at 3.3 Volts

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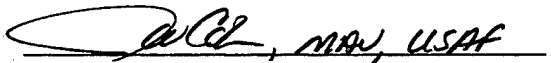

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Single Event Upset and Latchup Considerations for CMOS Devices Operated at 3.3 Volts

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Abstract A comparison of single event upset and latchup test results for devices operated at several bias levels, from 2.5V to 6V, is reported. Vulnerability to SEU increased with decreasing bias, whereas the opposite pattern was observed for SEL. The relationship between threshold SEU vulnerability and bias is not regular, which precludes the use of simple prediction schemes for obtaining the expected vulnerability at 3.3V from existing 5V data.

Introduction

In the past, the bias voltage (V_{DD}) applied to CMOS logic devices in satellite payloads has typically been held at about 5V. As a result, the majority of single event upset (SEU) and latchup (SEL) test data has been obtained at this voltage.[1] However, there has been a recent trend in consumer electronics toward reducing the bias voltage to 3.3V. Operation at 3.3V rather than 5V offers a number of advantages, the most obvious being reduced power consumption and heat generation. If other circuit characteristics (such as the signal to noise ratio and speed) are acceptable at reduced bias levels, then system operation at 3.3V provides a cost-effective alternative to 5V operation. The growing trend towards systems biased at 3.3V has also begun to influence space electronics systems, where power consumption is a vital concern. It is therefore important to assess the SEU and SEL vulnerabilities of CMOS devices at reduced bias voltage levels.

Previous studies have found that the SEU vulnerability of microcircuits increases with reduced bias voltage.[2,3] However, SEU data for bias levels near 3V are very scarce. In 1981, Kolasinski et al. tested two CMOS RAM device types at 3.5V and 4V (the devices were also tested at several increased bias levels, up to 9V). More recently, Roth et al., examined the SEU vulnerability of a single SRAM device type operated at between 2.5V and 6V, and concluded that the critical charge for upset varies linearly with the bias voltage. In contrast to the SEU vulnerability, the total dose performance is reportedly enhanced at reduced bias.[4]

The present study examines the SEU and SEL susceptibility of microcircuits operated at reduced bias levels ranging from 2.5V to 6V, and considers the particular implications of these results to 3.3V operation. Of primary interest is the question of whether or not test data obtained at higher bias levels can be extrapolated to lower levels such as 3.3V.

SEU Considerations

The tested device types are listed in Table 1. The test samples were fabricated by National Semiconductor in Fairchild's FACT™ technology; the feature size for these devices is 2 μm. Although the lot date codes indicate that the samples were manufactured in 1989, these devices are essentially the same as the functionally equivalent device types in National's more recent Low Voltage Logic (LVQ) Family, which have a recommended operating bias of 3.3V. The principal advantage of the FACT devices for SEU testing is the wide range of bias potentials, nominally 2.5V to 6V, at which they can be operated.

The devices listed in Table 1 were previously tested for SEU vulnerability at 5V.[5] The present study extends this work by characterizing, when possible, the SEU vulnerability at several bias voltages: 2.5V, 3.3V, 4V, 5V, and 6V. (Some device types did not operate either below about 2.5V or above about 6V.) Testing was performed at the Lawrence Berkeley Laboratory 88" cyclotron facility using Ar (180 MeV), Cu (290 MeV), Kr (380 MeV), and Xe (540 MeV) ions. The test methodology is described elsewhere.[6] SEU cross-section curves for several bias levels are presented in Figs. 1 through 4, respectively, for the four test device types listed in Table 1.

Table 1. SEU Test Samples

Device Type	Function	Date Code
54AC163	4-bit Binary Counter	8909
54ACT174	Hex D Flip-Flop	8920
54AC299	Octal Shift/Storage Register	8922
54ACT373	Octal Transparent Latch	8948

The threshold LET (linear energy transfer) of most devices decreased gradually as the bias voltage was reduced, as shown in Fig. 5. (The threshold LET was defined as the LET value at the point where the cross-section was about 5% of its saturation value.) However, the rate of decrease varied significantly from device type to device type. For example, 54AC163 displayed very little threshold dependence, whereas for 54ACT373 the threshold LET at 6V was nearly double the value at 2.5V. Furthermore, the relationship

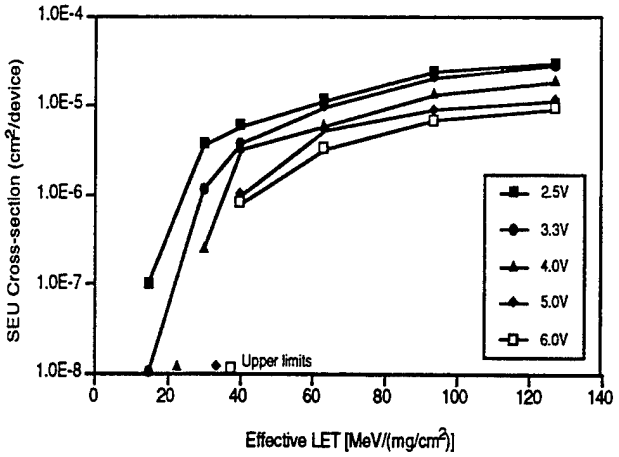

Fig. 1. SEU Test Results for 54AC163 at Several Bias Levels

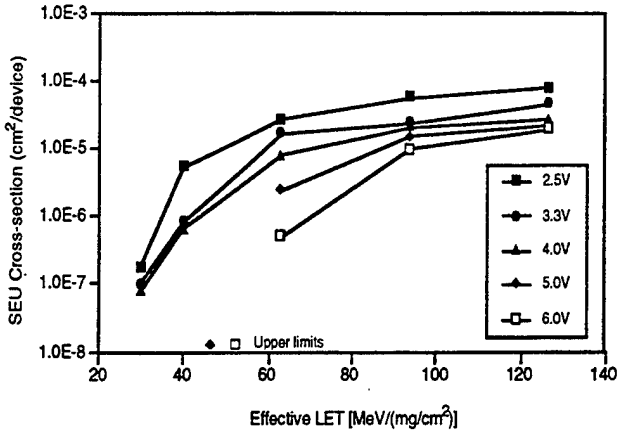

Fig. 3. SEU Test Results for 54AC299 at Several Bias Levels

between the bias and the threshold LET does not appear linear, nor, forthat matter, particularly regular. Notice, however, that the spread of threshold LET values is significantly smaller at reduced bias voltage than at higher levels. Thus, the variability in SEU susceptibility between device types belonging to the FACT family appears to be less at reduced bias levels.

SEL Considerations

The test device types listed in Table 1 were all immune to latchup, hence no SEL test data was obtained for these devices. The SEL study was instead carried out with a different device type, an ATMEL AT22V10B (CMOS PAL). Latchup susceptibility curves were obtained for this device at both 3V and 5V, as shown in Fig. 6. As can be seen, the latchup cross-section was substantially less in the reduced bias condition, especially at higher LETs. A similar test utilizing more bias levels (2V to 5V) was performed with a Toshiba TC5546 (8K x 8 CMOS SRAM). The test results, shown in Fig. 7, are consistent with the AT22V10B data.

Latchup is triggered by the formation of parasitic bipolar transistors in a CMOS circuit. The onset of latchup for AT22V10B is illustrated in Fig. 6. When the device underwent latchup (due to the passage of a single ion), the bias current increased to about 1,000 mA (see point D in Fig. 8). The irradiation was then halted, and the device current was gradually decreased, tracing the curve from D to C. The device remained in the latchup condition until point C (the holding point) was reached. The current was then decreased slightly, past the holding current, eliminating the latchup condition.

At lower bias voltages, the gain of the parasitic transistors and the amount of charge collected from an impinging ion both decrease. These factors contribute to the observed decrease in latchup susceptibility at reduced bias levels.

Other Single Event and Total Dose Effects

CMOS (and possibly NMOS circuits) are also susceptible to single event snapback (SES).[7] SES is caused by the activation of a parasitic n-p-n transistor in the n-channel. Since a reduction in the bias voltage decreases the necessary gain for the transistor, the likelihood of snapback formation is lessened at reduced bias levels. Problems due to breakdown of

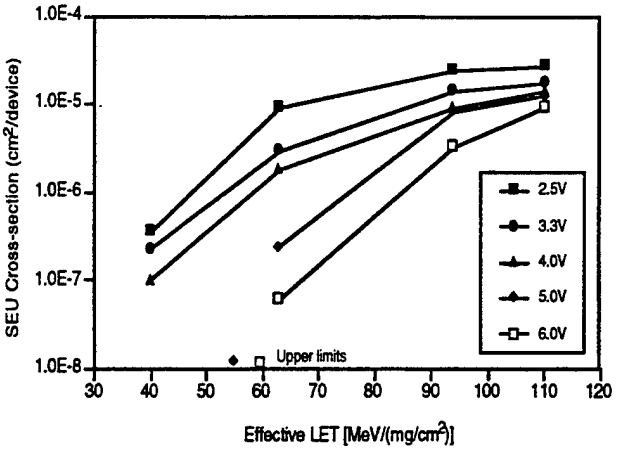

Fig. 2. SEU Test Results for 54ACT174 at Several Bias Levels

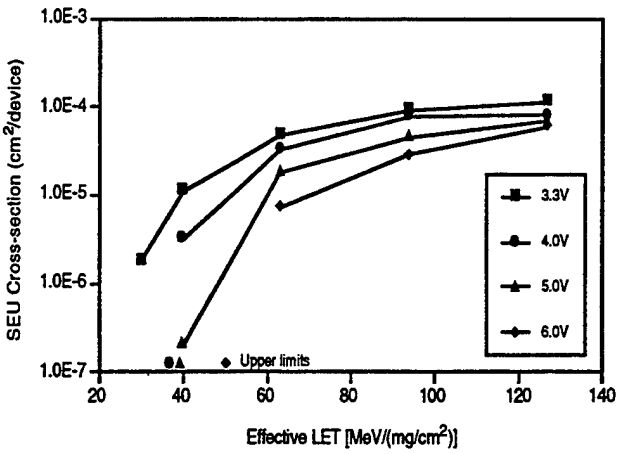

Fig. 4. SEU Test Results for 54ACT373 at Several Bias Levels

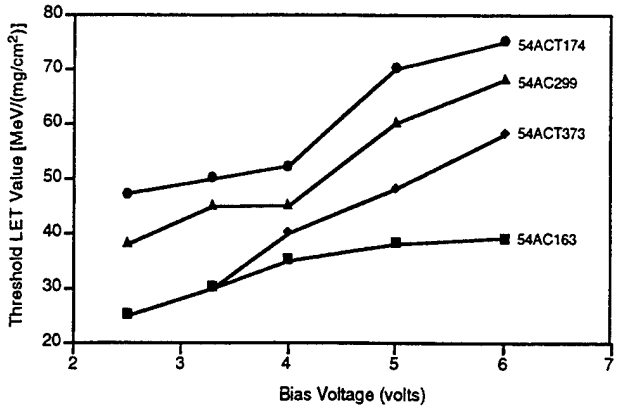

Fig. 5. SEU Threshold LET as a Function of Bias Voltage

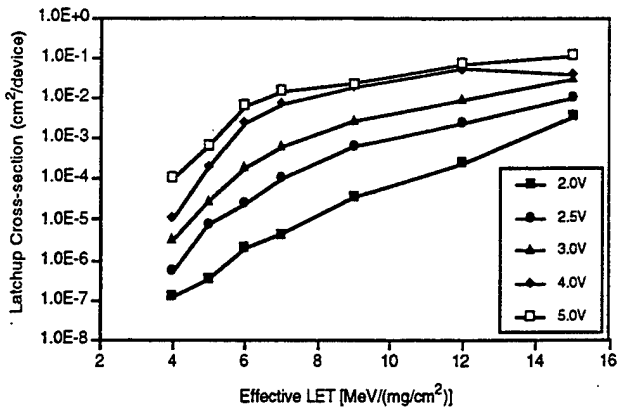

Fig. 7. Latchup Test Results for TC5546 at Several Bias Levels

parasitic bipolar transistors will also be lessened at reduced bias voltage.

The total ionizing dose limit of microcircuits has been shown to increase at reduced bias levels.[4] This is due to the reduced electrical field strength in the sensitive region, which increases the likelihood of electron-hole pair recombination (see below). For some devices, this total dose advantage is substantial.[4]

SEU Phenomenology

Charge collection is governed by the rate at which electrons and holes recombine after they are generated in (or near) the depletion region. Because the speed of charge carriers is essentially proportional to the electric field strength, a reduction in the field induces a proportional increase in the rate of charge recombination, hence reduced residual charge.

The thickness of the depletion region is approximately proportional to the square root of the applied field strength. Therefore, the volume in which the charge collection is effectively carried out is reduced by the square root of any reduction in the field strength.

To cause upset the collected charge must overcome the charge stored at the sensitive node. Because the stored charge is effectively proportional to the bias voltage, reducing the bias causes a proportional decrease in the critical charge.

Analytically then, one would expect the effect of reducing the bias voltage on the sensitive volume size to be small compared to the effect on the electron-hole recombination rate. In opposition to these effects is the decrease in stored charge at the sensitive node. The SEU test results reported above seem to indicate that the decreased critical charge predominates, hence the increased SEU susceptibility observed in the tests.

The upset thresholds obtained from SPICE simulations at various bias levels increase smoothly with increasing bias voltage, as shown in Fig. 9. However, it is not clear that SPICE successfully captures the subtle dependencies that exist in real-world interactions between charged particles and silicon devices. Detailed knowledge of device circuits is also needed to produce more realistic simulations.

Discussion

Present data indicate that CMOS devices operating at 3.3V will be more susceptible to SEU, but less vulnerable to latchup than those operating at 5V. Other high current anomalies, including snapback and possible breakdown, should also be reduced at lower bias levels.

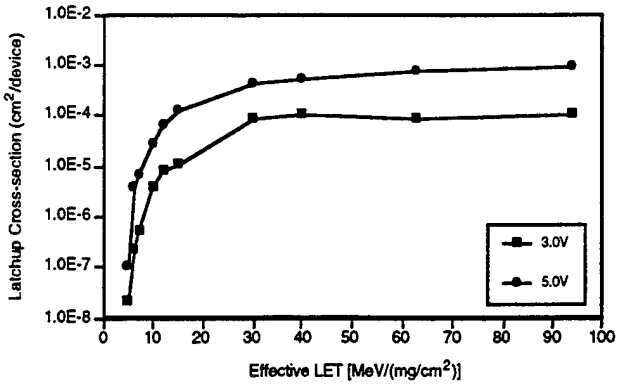

Fig. 6. Latchup Test Results for AT22V10B at Two Bias Levels

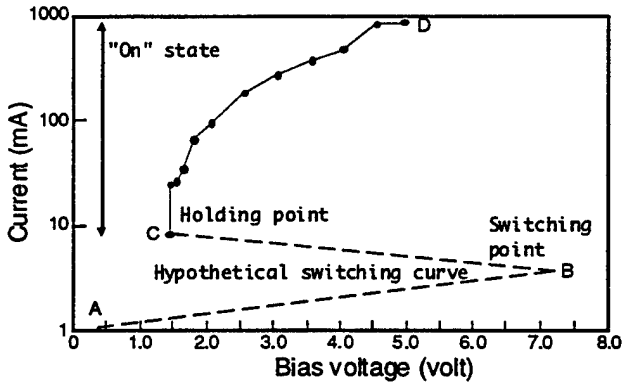

Fig. 8. Latchup Condition for AT22V10B

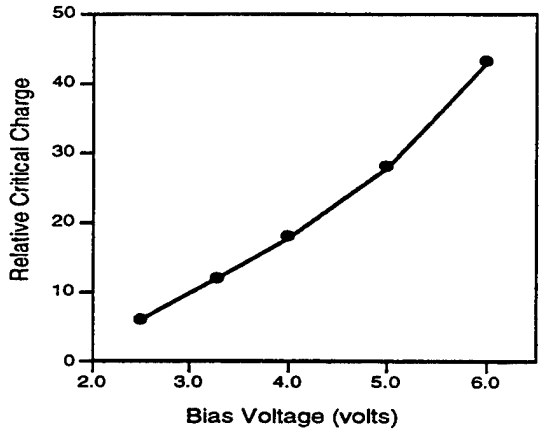

Fig. 9. Results of SPICE Simulations

The range of threshold LET values for devices in the FACT technology family was markedly compressed at 3.3V in comparison to 5V. This suggests that it may be possible to characterize the SEU vulnerability of an entire family of device types at 3.3V by testing only a few sample types.

However, the relationship observed between threshold LET and bias voltage was irregular, and varied from one device type to the next. For some device types the threshold increased relatively smoothly as the bias was increased, whereas others exhibited abrupt increases. Because of these irregularities, SEU results obtained at 5V cannot reliably be extrapolated to 3.3V.

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